In the specification:

Please amend paragraph 19 as follows:

FIG. 1 illustrates a front cross-sectional view of a first semiconductor wafer 4 and a second semiconductor wafer 7, in accordance with embodiments of the present invention. The first semiconductor wafer 4 comprises a topside 8 and a backside 10. The second semiconductor wafer 7 comprises a topside 12 and a backside 15. The term " topside" of a semiconductor wafer (e.g., topside 8 of the semiconductor wafer 4 and topside 12 of the semiconductor wafer 7) is defined herein including in the claims as a surface of a semiconductor wafer that comprises or will comprise (i.e., through a wafer/semiconductor device manufacturing process) active electrical components (e.g., transistors, resistors, capacitors, etc.) and/or conductive wiring between active electrical components. The term "backside" of a semiconductor wafer (e.g., backside 10 of the semiconductor wafer 4 and backside 15 of the semiconductor wafer 7) is defined herein including in the claims as a surface of a semiconductor wafer that does not comprise active electrical components (e.g., transistors, resistors, capacitors, etc.). The term "wafer/semiconductor device manufacturing process" is defined herein as a process to form a layer(s) of a material (i.e., for producing active electrical components, a mask, a junction (for transistors), an insulating layer, etc.) on a top side of a semiconductor wafer (e.g., topside 8 of the semiconductor wafer 4 and topside 12 of the semiconductor wafer 7). Any wafer/semiconductor device manufacturing process known to a person of ordinary skill in the art may be used for the present invention including, *inter alia*, diffusion, chemical vapor deposition (CVD) processing, etc. During a CVD process a furnace provides an environment comprising a high temperature (e.g., about 500°C to about 650°C) and a controlled gas 99 flow to form the layer(s)of a material. Gases 99 used during

a CVD process may include, *inter alia*, SiH4, nitrogen, etc. During diffusion process a furnace is used to expose the semiconductor wafer to an oxidizing environment at an elevated temperature (e.g., about 600°C to about 1300°C) to form the layer(s)of a material. Gases 99 used during a diffusion process may include, *inter alia*, oxygen, nitrogen, nitrous oxide, hydrogen, etc. During a wafer/semiconductor device manufacturing process, a layer formation (i.e., for producing active electrical components, a mask, a junction (for transistors), an insulating layer, etc.) on a first wafer (e.g., wafer 7) is modulated by a material (e.g., layer 21) that is adjacent to a topside (e.g., topside 12) of the first wafer (e.g., wafer 7) thereby producing values of an electrical characteristic(s) (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) that are dependent upon the material (e.g., layer 21). For example, the semiconductor wafer 4 comprises a film layer 21 of a specified material attached to the backside 10. The film layer 21 comprising the specified material may be selected by providing a relationship between a plurality of values for an electrical characteristic and a plurality of materials (see FIGS. 6-9). The relationship may be, *inter alia*, graphical (as shown in FIGS. 6 and 7), tabular, etc. The specified material comprised by the film layer 21 may be any material including, *inter alia*, Si, Si3N4, SiO2, etc. The gas 99 occupies an entire space 98 between film layer 21 and the topside12 of semiconductor wafer 7. The film layer 21 comprising the specified material is applied to the backside 10 of the semiconductor wafer 4 so that during the wafer/semiconductor device manufacturing process a desired value (i.e., a controlled value) of an electrical characteristic (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) for active electrical component(s) (e.g., transistors, resistors, capacitors, etc.) on the topside 12 of the semiconductor wafer 7 may be

obtained. Therefore specific discrete values for electrical characteristics of active electrical components (e.g., resistance (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) may be selected based upon specific materials selected (i.e., using the a relationship between a plurality of values for an electrical characteristic and a plurality of materials as shown in FIGS. 6 and 7). Based on a desired value for electrical characteristics of active electrical components, the film layer 21 (comprising a specific material) may be applied (i.e., coupled) to the backside 10 of the semiconductor wafer 4 prior to the wafer/semiconductor device manufacturing process as shown in FIG. 1. Alternatively a film layer may be removed (in a case where a semiconductor wafer comprises a plurality of film layers) to expose a film layer comprising a specific material as shown in FIGS. 2A and 2B.

Please amend paragraph 21 as follows:

FIG. 3 illustrates an alternative to FIGS. 1, 2A, and 2B showing a front cross-sectional view of a first semiconductor wafer 4, a second semiconductor wafer 7, and a filler wafer 28, in accordance with embodiments of the present invention. In contrast to FIGS. 1, 2A, and 2B, FIG. 3 comprises a filler wafer 28 (instead of a film layer (e.g., film layer 21 in FIG. 1 or film layer 24 in FIG. 2B) for producing the desired value (i.e., a controlled value) of an electrical characteristic (e.g., resistance such as polysilicon sheet resistance, capacitance, oxide thickness, threshhold voltage, standby current, etc) for active electrical component(s) (e.g., transistors, resistors, capacitors, etc.) on the topside 12 of the semiconductor wafer 7 during the wafer/semiconductor device manufacturing process. The filler wafer is placed between a backside 10 of the semiconductor wafer 4 and a topside 12 of the semiconductor wafer 7. The filler wafer 28 any

material including, inter alia, Si, Si3N4, SiO2, etc. The material used to produce the desired value is selected using the a relationship between a plurality of values for an electrical characteristic and a plurality of materials as shown in FIGS. 6 and 7. In FIG.3, the gas 99 (i.e., as described with reference to FIG. 1) occupies an entire space 98a between a first surface 77 of filler wafer 28 and the back side 10 of semiconductor wafer 7. Additionally, the gas 99 (i.e., as described with reference to FIG. 1) occupies an entire space 98b between a second surface 78 of filler wafer 28 and the topside 10 of semiconductor wafer 7.

Please amend paragraph 23 as follows:

If the method of FIG. 1 is selected in step 44 then step 50 is executed such that the film layer 21 (see FIG. 1) is applied (i.e., coupled) to the wafer 4 (such that the film layer 21 is ~~sandwiched~~ located between the topside 12 of the semiconductor wafer 7 and a backside 10 the semiconductor wafer 4). In step 52, the wafers 4 and 7 are placed in a furnace for a wafer/semiconductor device manufacturing process thereby producing a desired value (i.e., a controlled value) of an electrical characteristic (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) for active electrical component(s) (e.g., transistors, resistors, capacitors, etc.) on the topside 12 of the semiconductor wafer 7.